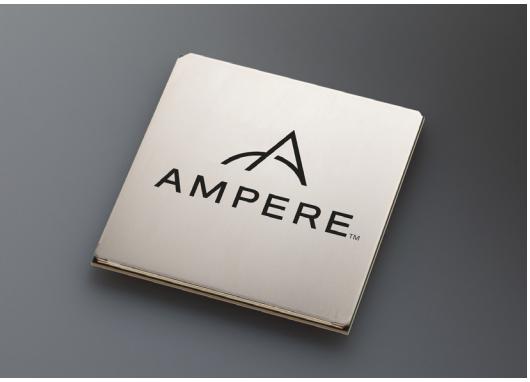
AMPERE™



Ampere 64-bit Arm Processor

The Ampere 64-bit, custom designed, multicore processor targets the future of the data center by providing a large number of high-performance cores, high-memory bandwidth and capacity, general purpose high-bandwidth I/O and a high level of integration—within an efficient power envelope.

Features

PROCESSOR SUBSYSTEM

- 32 Arm v8 64-bit CPU cores up to 3.3 GHz with Turbo
- 32 KB L1 I-cache, 32 KB L1 D-cache per core
- Shared 256 KB L2 cache per 2 cores

MEMORY

- 32 MB globally shared L3 cache
- 8x 72-bit DDR4-2667 channels
- Advanced ECC and DDR4 RAS features
- Up to 16 DIMMs, 1 TB/socket

SYSTEM RESOURCES

- Full interrupt virtualization
- I/O virtualization
- Enterprise server-class RAS
  - End-to-end data poisoning
  - Error containment and isolation
  - Background L3 and DRAM scrubbing

CONNECTIVITY

- 42 lanes of PCIe Gen 3, with 8 controllers
  - x16 or two x8/x4
  - x16 or two x8/x4
  - x8 or two x4
  - Two x1
- 4 x SATA Gen 3 ports
- 2 x USB 2.0 ports

Next-generation data centers and cloud deployments are driving accelerating demand for higher compute performance, larger memory capacity and greater memory bandwidth, all at lower power and cost.

The Ampere 64-bit multi-core processor is custom built for large-scale public and private cloud environments. It supports accelerated delivery and deployment of cloud workloads within a power envelope of 125 W. The device also features enterprise grade Reliability, Availability and Serviceability (RAS) capabilities and Arm® server standards compliance, providing an overall substantial reduction in the Total Cost of Ownership (TCO).

CPU Memory Sub-System

The Ampere processor features 32 high-performance 64-bit Arm v8.0-A CPU running at up to 3.3 GHz with Turbo mode support. The cache sub-system includes a 3-level hierarchy with a 32 MB last level L3 cache that is available to all 32 cores in the system. With eight DDR4-2667 memory channels, the device delivers superior memory bandwidth and up to 1 TB of memory capacity across 16 DIMMs. These attributes make it well suited for all cloud workloads in a variety of areas including the web tier, data analytics, big data and storage.

I/O and Connectivity

The Ampere processor provides I/O expansion via PCIe Gen 3. The device features 42 PCIe Gen 3 lanes with 8 individual controllers that could be used for networking, storage or accelerator connectivity. The 42 lanes can be configured as PCIe x16 or x8 or x4 or x1. This provides flexibility for PCIe add-on networking cards up to 100GbE or more, and storage expanders or NVME storage devices, making it well suited for big data applications. The PCIe x16/x8 controllers can also be used for external accelerator connectivity to FPGAs, ASICs, GPUs and more.

In addition, the device features built-in SATA ports for storage, USB ports for expansion and a 1 GbE network port for LAN on motherboard connectivity.

Virtualization

The Ampere processor provides full CPU and I/O virtualization support for running workloads and applications within virtual machines, an increasingly prevalent model in the cloud.

Security and Power Management

The Ampere processor integrates dedicated microcontrollers for power and system management. The advanced power management capabilities include Advanced Configuration Power Interface (ACPI) v6.x support as well as Dynamic Frequency Scaling (DFS), on-die thermal monitoring, dynamic power estimation and Turbo mode support. The system management features include platform management, secure boot and interface to an external Baseboard Management Controller (BMC).

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Features (cont.)

TECHNOLOGY & FUNCTIONALITY

- TSMC 16 nm FinFET+
- Arm v8.0-A, SBSA Level 3
  - EL3, secure memory and secure boot support
- Advanced power management

POWER

- TDP: 125 W

Reliability, Availability and Serviceability (RAS)

The Ampere processor provides extensive enterprise server class RAS capabilities. Data in memory is protected with advanced ECC in addition to standard DDR4 RAS features. End-to-end data poisoning ensures corrupted data is tagged and any attempt to use it is flagged as an error. The large L3 cache is also ECC protected, and the processor supports background scrubbing of the L3 cache and DRAM to locate and correct single-bit errors before they accumulate into uncorrectable errors.

Technology and Compliance

The Ampere processor is fabricated using TSMC's proven 16 nm FF+ high-performance process technology. The device is fully compliant with the Arm server SBSA and SBBR standards.

Block diagram